University of Virginia
Charles L. Brown Department of Electrical and Computer Engineering

ECE 3663: Digital Integrated Circuits
Design Project Assignment

Spring 2012

Issued: 02/02/12
Form Group: 02/14/12
Design Review 1 Due: 03/13/12
Design Review 2 Due: 04/10/12
Final Report Due: 04/24/12
Presentation Due: 04/24/12

You work on a design team (4 people) for a startup company that specializes in digital IC design. Your team has learned of the opportunity to win a large contract from Portable Instruments Company (PICo) to develop an embedded Digital Signal Processor design in the FreePDK 45nm technology. In order to win the contract, your team must design and implement a proof of concept circuit block and demonstrate it using simulation. You will be competing with teams from other companies to win the contract. Prof. Calhoun is the liaison to your group from PICo who will evaluate your design.

Design Description
The figure below illustrates the basic structure of the DSP block that you must design:

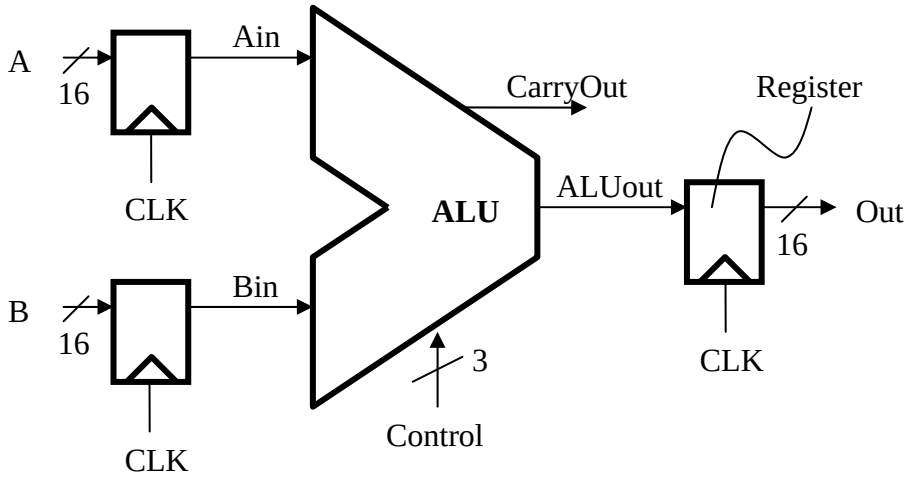

Figure 1 – The DSP system that you must design to compete for the PICo contract.

The ALU must be able to compute the following functions, as defined by your control bits (you may choose the assignment of control bits to functions):

ALU Function	**Description**
NOP	Do nothing – No change at Out
ADD	Out = A + B
SUB	Out = A - B
SHIFT	Out = A << B
AND	Out = A & B
OR	Out = A | B
Pass A	Out = A
Arbitrary	Out = <function of your choice>

Deliverables:
You must deliver a complete transistor level hierarchical schematic and/or netlist of the entire DSP (including the registers) as shown in Figure 1. You must convince the PICo board that your design works by demonstrating proper functionality of all functions using Cadence simulations.
The PICo board will select the function design that exhibits the lowest design metric given by: Metric = (Active Power)*Delay^2*Area, and taking into account the special feature.

Specification
For the metric, the *active power* is measured for one computation per cycle at the highest frequency achievable by the design for a specific series of inputs, which PICo will supply at the second design review. The *delay* is the worst case access delay. The *area* is the sum of the widths of transistors used in the design.

You may assume that your design will interface with pads that connect to the outside world (you do not have to design the pads). All **inputs** are valid 0.5 FO4 (fan out of 4) delay before the rising edge of the clock and hold for 1 FO4 delay after the rising edge of the clock. You may assume that the clock is an ideal signal driven through a static CMOS buffer (e.g. series inverters) of a size of your choice (include the buffer in your final simulations).

Special Feature
Your team must design and implement a single arbitrary function in the ALU, and the quality/complexity of that arbitrary function will give your design an advantage in the final comparison with other teams. Consult with Prof. Calhoun about your ideas for the arbitrary function.

Graded Elements: Your project grade is based on the following four components. All of these components are delivered by the group.

1) Create and update your group's page on the wiki to describe your project and your results (ongoing assignment). Create your group page and link off the bottom of the class main page:
https://venividiwiki.ee.virginia.edu/mediawiki/index.php/ClassECE3663Spring12

2) Design reviews – Due March 13, and April 10 – Each design review is intended to give you a chance to update the PICo review board of your progress and to get feedback and suggestions. You will turn in hard copies of simulations and/or schematics to show your progress. You will also turn in a 1 page typed description of your group's progress and of the remaining tasks. The final design review (due April 24th) will accompany the Final Report and Final Presentation. *You will receive separate assignments related to each design review to give more details.*
To give you an idea of the expected progress, the following minimum levels of functionality must be demonstrated:
Design Review 1 – AND, OR, PASS A, 8:1 Mux
Design Review 2 – ADD, SUB, SHIFT, ALU in/out connectivity, registers working

3) Final Report – Due April 24 – Turn in a 4 page conference-style paper describing your project. A template will be available to show the format.

4) Final Presentation – Slides Due April 24 – Your group will present your results to the class in a conference-style presentation using slides.

You may ask questions about the project at:
https://venividiwiki.ee.virginia.edu/mediawiki/index.php/ClassECE3663Spring12ProjectQA

You should also check this page to look at answers (given by PICo) to other teams' questions.

Group Selection
Select 1 partner and email Prof. Calhoun both of your names BEFORE Feb 14. Prof. Calhoun will assign the teams.